Instruction Manual

Tektronix

TMS708
MSC8101 Microprocessor Software Support

071-1117-00

www.tektronix.com

Tektronix, Inc., P.O. Box 500, Beaverton, OR 97077

SOFTWARE WARRANTY

Tektronix warrants that the media on which this software product is furnished and the encoding of the programs on the media will be free from defects in materials and workmanship for a period of three (3) months from the date of shipment. If a medium or encoding proves defective during the warranty period, Tektronix will provide a replacement in exchange for the defective medium. Except as to the media on which this software product is furnished, this software product is provided “as is” without warranty of any kind, either express or implied. Tektronix does not warrant that the functions contained in this software product will meet Customer’s requirements or that the operation of the programs will be uninterrupted or error-free.

In order to obtain service under this warranty, Customer must notify Tektronix of the defect before the expiration of the warranty period. If Tektronix is unable to provide a replacement that is free from defects in materials and workmanship within a reasonable time thereafter, Customer may terminate the license for this software product and return this software product and any associated materials for credit or refund.

THIS WARRANTY IS GIVEN BY TEKTRONIX IN LIEU OF ANY OTHER WARRANTIES, EXPRESS OR IMPLIED. TEKTRONIX AND ITS VENDORS DISCLAIM ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE. TEKTRONIX’ RESPONSIBILITY TO REPLACE DEFECTIVE MEDIA OR REFUND CUSTOMER’S PAYMENT IS THE SOLE AND EXCLUSIVE REMEDY PROVIDED TO THE CUSTOMER FOR BREACH OF THIS WARRANTY. TEKTRONIX AND ITS VENDORS WILL NOT BE LIABLE FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES IRRESPECTIVE OF WHETHER TEKTRONIX OR THE VENDOR HAS ADVANCE NOTICE OF THE POSSIBILITY OF SUCH DAMAGES.

Table of Contents

Reference

Specifications

Replaceable Parts List

Index

List of Figures

List of Tables

Preface

This instruction manual contains information specific to the TMS708 MSC8101 microprocessor support package and is part of a set of information on how to operate this product on compatible Tektronix logic analyzers.

If you are familiar with operating microprocessor support packages on the logic analyzer for which the TMS708 MSC8101 support was purchased, you will probably only need this instruction manual to set up and run the support.

If you are not familiar with operating microprocessor support packages, you will need to supplement this instruction manual with information on basic operations to set up and run the support.

Information on basic operations of microprocessor support packages is included with each product. Each logic analyzer includes basic information that describes how to perform tasks common to support packages on that platform. This information can be in the form of online help, an installation manual, or a user manual.

This manual provides detailed information on the following topics:

- Connecting the logic analyzer to the target system
- Setting up the logic analyzer to acquire data from the target system
- Acquiring and viewing cycle type labels

Manual Conventions

This manual uses the following conventions:

- The term “disassembler” refers to the software that decodes bus cycles and displays cycle types.
- The phrase “information on basic operations” refers to the logic analyzer online help, an installation manual, or a user manual covering the basic operations of the microprocessor support.
- The term “logic analyzer” refers to the Tektronix logic analyzer for which this product was purchased.

Contacting Tektronix

Phone	1-800-833-9200*
Address	Tektronix, Inc. Department or name (if known) 14200 SW Karl Braun Drive P.O. Box 500 Beaverton, OR 97077 USA
Web site	www.tektronix.com
Sales support	1-800-833-9200, select option 1*
Service support	1-800-833-9200, select option 2*
Technical support	Email: techsupport@tektronix.com 1-800-833-9200, select option 3* 6:00 a.m. - 5:00 p.m. Pacific time

* **This phone number is toll free in North America. After office hours, please leave a voice mail message.**
Outside North America, contact a Tektronix sales office or distributor; see the Tektronix web site for a list of offices.

Getting Started

Getting Started

This section contains information on the TMS708 MSC8101 microprocessor support, and information on connecting your logic analyzer to your target system.

Support Package Description

The TMS708 microprocessor support package displays the Cycle Type labels, marks the Idle Cycles, and validates the data bus and the address bus. The TMS708 does not display the instructions nor identify the Fetch cycles. The Motorola MSC8101 16-bit Digital Signal Processor (DSP) is the first member of the family of DSPs based on the Starcore SC140 DSP core.

The TMS708 installs two support packages 8101_SNG and 8101_MLT.

- 8101_SNG supports the Single Master mode of MSC8101 processor.
- 8101_MLT supports the Multi Master mode of MSC8101 processor. You can use the 8101_MLT support for Internal and External Arbiter configurations. In the Internal Arbiter configuration, the software supports three more external masters on the same system bus. In the External Arbiter configuration, the software supports up to four masters. The software decodes the cycles of all the masters.

The TMS708 microprocessor support package decodes the Cycle Types, validates the data bus and identifies the Idle Cycles. The support does not decode Instructions.

Refer to information on basic operations to determine how many modules and probes your logic analyzer needs to meet the minimum channel requirements for the TMS708 microprocessor support.

To use this support efficiently, you need the items listed in the information on basic operations as well as the MSC8101 Microprocessor User Manual (Motorola, April 2001, and Revision 0, MSC8101RM/D).

Logic Analyzer Software Compatibility

The label on the microprocessor support floppy disk states which version of logic analyzer software this support is compatible with.

Logic Analyzer Configuration

The TMS708 MSC8101 microprocessor support requires the following minimum module configuration:

- One 136-channel, 100 MHz module for 8101_SNG support
- One 136-channel, 100 MHz module for 8101_MLT support

Requirements and Restrictions

Review the electrical specifications in the *Specifications* section in this manual as they pertain to your target system, as well as the following descriptions of other MSC8101 support requirements and restrictions.

Hardware Reset. If a hardware reset occurs in your MSC8101 system during an acquisition, the disassembler application might acquire invalid samples.

System Clock Rate CLKOUT. The support can acquire data from the MSC8101 microprocessor operating at speeds of up to 100 MHz[1]. The 8101_SNG support has been tested for speeds up to 50 MHz and the 8101_MLT support up to 66MHz.

T_Code Group in 8101_MLT Group. The T_Code channel group consists of signals TC0/BR0~, TC1/BG0~, and TC2/DBG0~. By default, this group is hidden in the support package. If you want to use the support for Internal Arbiter Configuration, you must connect the signals TC0, TC1, and TC2 to the logic analyzer channels C0:1, C0:0 and C2:6. To view the activities of TC[0-2] signals, add the T_Code group to the listing using CTRL+L. If you want to use the support for External Arbiter configuration, connect the signals BR0~, BG0~, and DBG0~ to the logic analyzer channels C0:1,C0:0, and C2:6. The T_Code group is not valid in External Arbiter Configuration.

Triggering on Address in a Burst Transaction. The signals BADDR[31–27] generate the address increments to memory devices for burst accesses and these are not visible when signals A[31–27] are connected to the logic analyzer channels A0:[0–4]. You can trigger on an address within a burst transaction only if signals BADDR[31–27] are connected to the logic analyzer channels A0:[0–4]. The disassembler displays the address increments for burst transactions even though signals A[31–27] are probed.

1 Specification at time of printing. Contact your Tektronix sales representative for current information on the fastest devices supported.

Signals Not Required in the Channel Assignment. The TMS708 MSC8101 support package decodes cycle types, validates address and data bus, and identifies the idle cycles acquired by clock-by-clock acquisition. It does not decode instructions. The channel assignment contains signals that are not required to support cycle type decoding, validate address and data bus, or identify idle cycles. If you include the P6434 high-density probe interface in your design, we recommend that you use these signals.

EAV Bit Setting in 8101_SNG Support. Set the EAV (Enable Address Visibility) bit of the Bus Configuration Register (BCR) to 1 for correct disassembly. When the EAV is set to 1, the Bank Select signals are not driven on the address bus. During READ and WRITE commands to SDRAM devices, the full address is driven on bus address lines. Therefore, when the EAV bit is set to 1, the full address is valid at PSDCAS~ asserted and PSDRAS~ deasserted for SDRAM accesses.

Qualifiers Used in 8101_MLT Support. The Multi Master support uses the internal memory controller signals for validating Address and Data. The support uses the ALE signal to qualify a valid Address and the PSDVAL~ signal to qualify a valid data on the bus. The external masters connected to the system may be an MSC8101 or a non-MSC8101processor. For an MSC8101 processor, the ALE and PSDVAL~ signals are the qualifiers. For a non-MSC8101 processor, the ALE and TA~ signals are the qualifiers.

Address Pipelining. The TMS708 support is designed to support pipelining up to one level. While acquiring data from systems with pipelining, you may at the beginning acquire data tenures without any corresponding address tenures. The support, by default, starts associating the first data with the first acquired address tenure. This may cause incorrect Cycle Type decoding. In that case, you must associate the first acquired address with the correct data tenure using the ‘Invalid Data’ marking option. You must mark as ‘Invalid Data’ the first data tenure without any corresponding address. Once you mark the Invalid Data, the support package adjusts itself to associate the address and data correctly.

Nonintrusive Acquisition. Acquiring microprocessor bus cycles is nonintrusive to the target system. That is, the TMS708 MSC8101 microprocessor does not intercept, modify, or present back signals to the target system.

Channel Groups. The channel groups required for clocking and cycle type decoding in the 8101_SNG support are:

Address
Hi_Data
Lo_Data
Control
Chip_Sel
Byte_Enb
Misc

The channel groups required for clocking and cycle type decoding in the 8101_MLT support are:

Address
Hi_Data
Lo_Data
Control
Chip_Sel
T_Type
T_Size
T_Code
Req_Grant

Timing Display Format

The support has a Timing Display Format file. It sets up the display to show the following waveforms:

For 8101_SNG Support:

CLKOUT
Address
Hi_Data
Lo_Data
PSDRAS~/POE~
PSDCAS~
PSDVAL~
Control
Chip_Sel
Byte_Enb
Misc

NOTE. *The Address, Hi_Data, Lo_Data, Control, Chip_Sel, Byte_Enb, and Misc groups are displayed in busform.*

For 8101_MLT Support:

CLKOUT
Address
Hi_Data
Lo_Data
TS~
ALE
TA~
TEA~
AACK~
PSDVAL~
T_Type
T_Size
T_Code
Control
Chip_Sel
Req_Grant

***NOTE**. The Address,Hi_Data, Lo_Data, T_Type, T_Size, T_Code, Control, Chip_Sel, and Req_Grant groups are displayed in busform.*

Functionality Not Supported

The TMS708 software does not support the following functionalities:

- UPM cycles
- DMA cycles
- HDI16 cycles
- Multiple master mode with multiple memory controllers
- PowerPC local bus cycles

Functionality Supported But Not Tested

The TMS708 software supports the following features, but are not tested.

- 60X system bus interface of the MSC8102 processor
- External Arbiter Configuration in 8101_MLT support
- Atomic bus operations (RAWA, WARA) in 8101_SNG support

Connecting the Logic Analyzer to a Target System

You can use the channel probes, clock probes, and leadsets with a commercial test clip (or adapter) to make the connections between the logic analyzer and your target system.

To connect the probes to MSC8101 signals in the target system using a test clip, follow the steps:

1. Power off your target system. You do not need to power off the logic analyzer.

CAUTION. *To prevent static damage, handle the microprocessor, probes, and the logic analyzer module in a static-free environment. Static discharge can damage these components.*

Always wear a grounding wrist strap, heel strap, or similar device while handling the microprocessor.

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. If you are using a test clip, touch any of the ground pins on the clip to discharge stored electricity from the test clip.

CAUTION. *To prevent permanent damage to the pins on the microprocessor, place the target system on a horizontal surface before connecting the test clip.*

3. Place the target system on a horizontal, static-free surface.
4. Use Tables 3-27 through 3-34 starting on page 3-21 to connect the channel probes to MSC8101 signal pins on the test clip or in the target system.
5. Use leadsets to connect at least one ground lead from each channel and the ground lead from each clock probe to the ground pins on your test clip.

Labeling P6434 Probes

The TMS708 MSC8101 software support package relies on the channel mapping and labeling scheme for the P6434 Probes. Apply labels using the instructions described in the P6434 Probe Instructions manual.

Operating Basics

Setting Up the Support

This section provides information on how to set up the support and covers the following topics:

- Installing the support software
- Channel group definitions
- Clocking options

The information in this section is specific to the operations and functions of the TMS708 MSC8101 support on any Tektronix logic analyzer for which the support can be purchased. Information on basic operations describes general tasks and functions.

Before you acquire and display cycle type labels, you need to load the support and specify the setups for clocking and triggering as described in the information on basic operations. The support provides default values for each of these setups, but you can change the default values as needed.

Installing the Support Software

***NOTE**. Before you install any software, you should verify that the microprocessor support software is compatible with the logic analyzer software.*

To install the TMS708 MSC8101 software on your Tektronix logic analyzer, follow these steps:

1. Insert the floppy disk in the disk drive.
2. Click the Windows Start button, point to Settings, and click Control Panel.
3. In the Control Panel window, double-click Add/Remove Programs.
4. Follow the instructions on the screen for installing the software from the floppy disk.

To remove or uninstall software, follow the above instructions and select Uninstall. You need to close all windows before you uninstall any software.

Channel Group Definitions

The software automatically defines channel groups for the support.

8101_SNG Support

The channel groups for the TMS708 8101_SNG support are: Address, Hi_Data, Lo_Data, Control, Chip_Sel, Byte_Enb, and Misc. Table 2–1 shows the channel groups and the display radix for the 8101_SNG support.

Table 2–1: Channel groups for the Single Master Mode

Group name	Display radix
Address	HEX
Hi_Data	HEX
Lo_Data	HEX
Mnemonics	NONE (disassembler generated text)
Control	SYM
Chip_Sel	SYM
Byte_Enb	SYM
Misc	HEX (hidden by default)

8101_MLT Support

The channel group for the TMS708 8101_MLT support are: Address, Hi_Data, Lo_Data, T_Type, T_Size, T_Code, Control, Chip_Sel, and Req_Grant. Table 2–2 shows the channel groups and the display radix for the 8101_MLT support.

***NOTE**. The T_Code group is applicable only in Internal Arbiter Mode.*

Table 2–2: Channel groups for the Multi Master Mode

Group name	Display radix
Address	HEX
Hi_Data	HEX
Lo_Data	HEX
Mnemonics	NONE (disassembler generated text)
Control	SYM (hidden by default)
Chip_Sel	SYM
T_Type	SYM
T_Size	SYM
T_Code	SYM (hidden by default)
Req_Grant	SYM

If you want to know which signal is in which group, refer to the channel assignment tables beginning on page 3–7.

Clocking

Acquisition Setup

The TMS708 MSC8101 affects the logic analyzer setup menus (and submenus) by modifying existing fields and adding micro-specific fields.

On the logic analyzer, the TMS708 MSC8101 support adds the selection '8101_SNG' and '8101_MLT' to the Load Support Package dialog box, under the File pulldown menu. Once 'TMS708 MSC8101 support' is loaded, the 'Custom' clocking mode selection in the logic analyzer module Setup menu is also enabled.

Clocking Options

The TMS708 support offers a microprocessor-specific clocking mode for the MSC8101 microprocessor. This clocking mode is the default selection whenever you load the MSC8101 support.

The disassembly will not be correct when using the Internal or External clocking modes. Information on basic operations describes how to use these clock selections for general purpose analysis.

Custom Clocking

A special clocking program is loaded to the module every time you load the 8101_SNG or 8101_MLT support. This special clocking is called Custom.

With Custom Clocking, the module logs in signals from the multiple channel groups at every clock on the TMS708 MSC8101 bus. The module then sends all the logged-in signals to the trigger machine and stores the signals in the acquisition memory of the module.

When Custom is selected, the Custom Clocking Options menu adds the subtitle: '8101_SNG Microprocessor Clocking Support' or '8101_MLT Microprocessor Clocking Support', and displays the clocking option—Standard. This is the only custom clocking option available for this support.

Acquiring and Viewing Disassembled Data

This section describes how to acquire and view data. The following information covers these topics and tasks:

- Acquiring data
- Viewing cycle type labels
- Changing the way labels are displayed
- Timing diagrams

Acquiring Data

The TMS708 MSC8101 software package installs the 8101_SNG support for the MSC8101 processor working in Single Master mode and the 8101_MLT for MSC8101 processor working in Multi Master mode (for up to four masters on the target system). Once you load the support, by default, the custom clocking option is selected. Specify the trigger, if any, and you are ready to acquire and disassemble data.

If you have any problems acquiring data, refer to information on basic operations in your online help or *Appendix A: Error Messages and Disassembly Problems* in the user manual.

Signal Acquisition

8101_SNG Support. The Custom Clock uses the falling edge of the CLKOUT signal.

Figures 2-1 and 2-2 show the Bus Timing diagrams for SDRAM memory and GPCM memory in the Single Master mode.

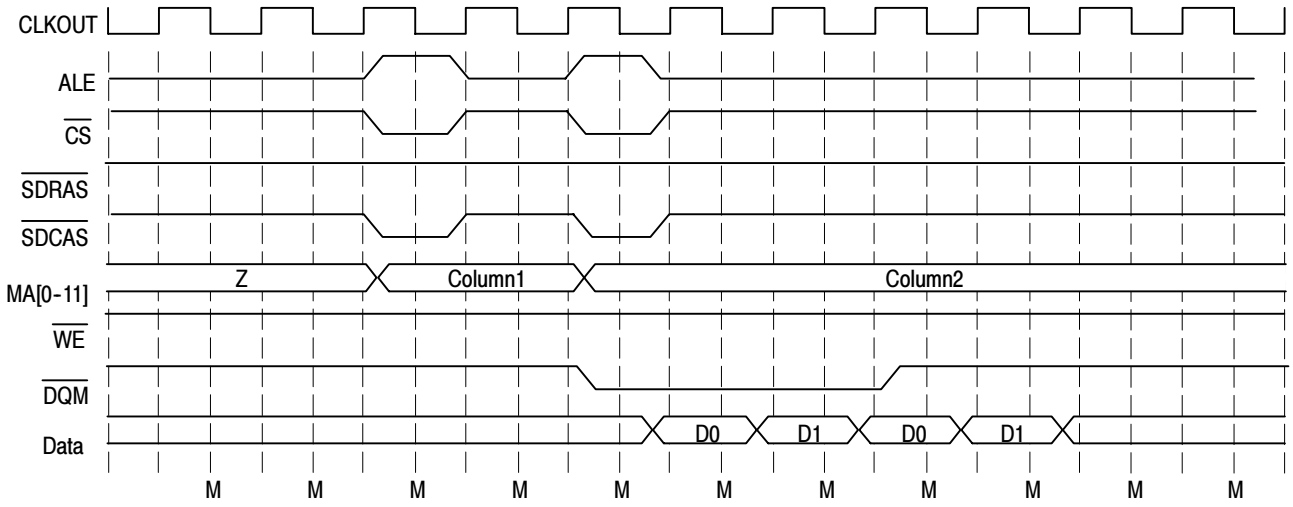


Figure 2-1: Bus timing diagram for SDRAM memory

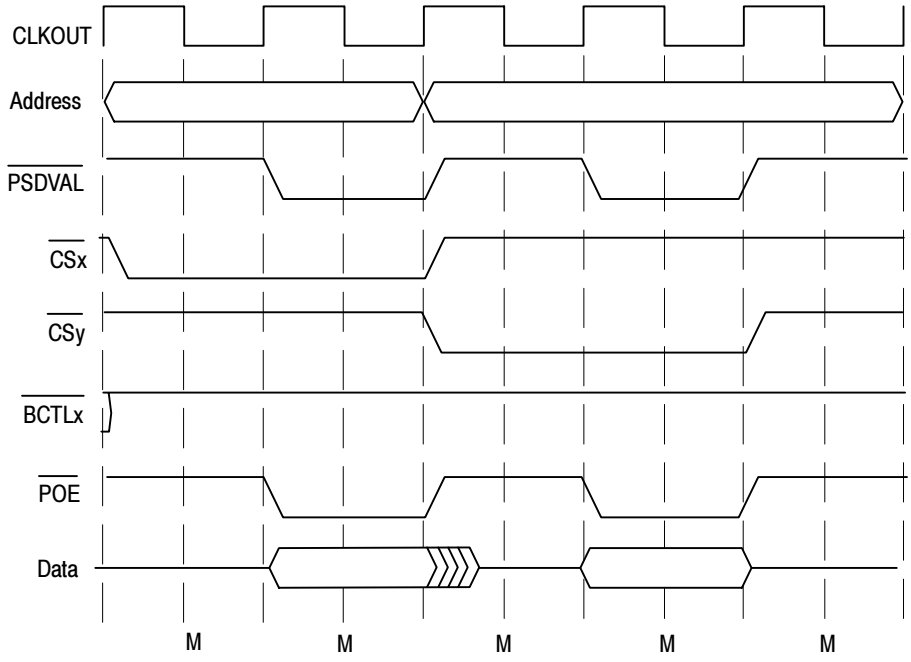


Figure 2-2: Bus timing diagram for GPCM memory

Table 2-3 describes the sample points in 8101_SNG support.

Table 2-3: Sample points in Single Master Mode

Sample point	Signals
Master sample point, M	A[0-31], D[0-31], D[32-63], CS~[0-7], PWE~[0-7], PSDCAS~, PSDRAS~/POE~, PSDVAL~, CLKOUT, PSDWE~, PSDA10, PGTA~, PSDAMUX, BCTL0~, BCTL1~, NMI_OUT, HRESET~, SRESET~, PORESET~, NMI~, DP6~/DACK3~, DP7~/DACK4~, IRQ7~/INT_OUT~

The only sample point is M (Master). All the signals are logged and mastered at every falling edge of the CLKOUT signal.

8101_MLT Support. The Custom Clock uses the rising edge of the CLKOUT.

Figure 2-3 shows the Bus Timing diagram for Multi Master mode.

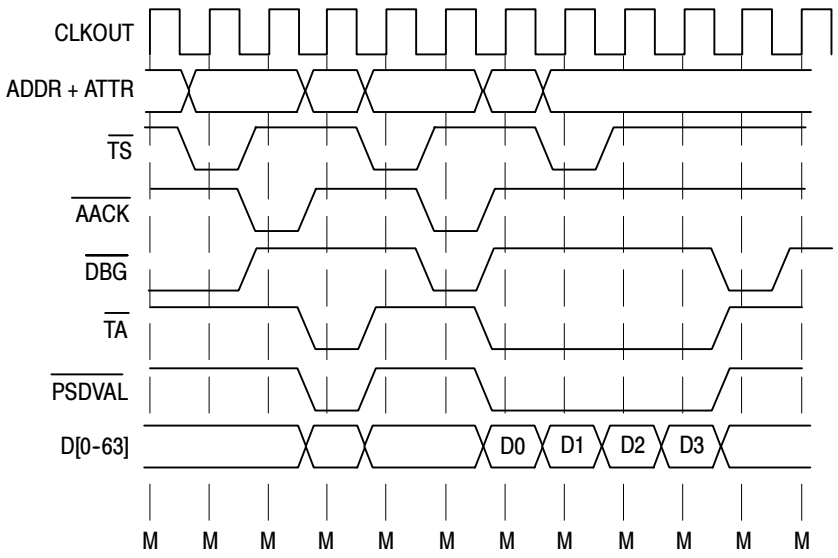


Figure 2-3: Bus timing diagram for Multi Master mode

Table 2-4 describes the sample points in 8101_MLT support.

Table 2-4: Sample points in Multi Master Mode

Sample point	Signals
Master sample point, M	A[0-31], D[0-31], D[32-63], CS~[0-7], TS~, CLKOUT, PSDVAL~, AACK~, ABB~, BG~, DP0~/EXT_BR2~, BR~, ALE, DBG~, DBB~, TC0/BR0~, TC1/BG0~, TC2/DBG0~, TT[0-4], TSIZ[0-3], DP3~/EXT_BR3~, DP1~/EXT_BG2~, DP2~/EXT_DBG2~, DP4~/EXT_BG3~, TBST~, ARTRY~, DP5~/EXT_DBG3~, TA~, TEA~

The only sample point is M (Master). All the signals are logged and mastered at every rising edge of the CLKOUT signal.

Viewing Cycle Type Labels

You can view cycle type labels only in the Hardware display format. The information on basic operations describes how to select the disassembly display formats.

***NOTE**. You must set the selections in the Disassembly property page (the Disassembly Format Definition overlay) correctly for your acquired data to be disassembled correctly. Refer to* Changing How Labels are Displayed *on page 2-13.*

For the 8101_SNG support, the default display format shows the Address, Hi_Data, Lo_Data, Mnemonics, Control, Chip_Sel, Byte_Enb channel group values for each sample of acquired data.

For the 8101_MLT support, the default display format shows the Address, Hi_Data, Lo_Data, Mnemonics, T_Type, T_Size, Chip_Sel channel group values for each sample of acquired data.

If a channel group is not visible, you can add the required column by pressing Ctrl + L and selecting the group of interest.

Table 2–5 shows the special characters and gives a definition of what they represent.

Table 2–5: Description of special characters in display

Character or string displayed	Description
>>	The sample was manually marked

Hardware Display Format

In the Hardware display format, the support displays all cycle type labels in parentheses.

In Hardware display format, all cycle type labels are displayed. This is the default format for viewing the data.

Tables 2–6 and 2–7 show the cycle type labels and their descriptions that the support recognizes and displays.

Table 2–6: Cycle type label definitions for the 8101_SNG support

Cycle type	Definition
(SDRAM-Activate Cycle)	Indicates a SDRAM Activate command
(SDRAM-Precharge Cycle)	Indicates a SDRAM Precharge command
(SDRAM-Refresh Cycle)	Indicates a SDRAM Refresh command
(Row Address)	Indicates the presence of Row Address on the Address bus
(Column Address)	Indicates the presence of Column Address on the Address bus
(SDRAM-Read Cycle)	Indicates a SDRAM Read cycle
(SDRAM-Write Cycle)	Indicates a SDRAM Write cycle
(Hardware Reset Cycle)	Indicates a Hardware Reset Operation
(Software Reset Cycle)	Indicates a Software Reset Operation
(Power On Reset Cycle)	Indicates a Power On Reset Operation
(SDRAM Fetch)	Indicates a Fetch Cycle
(Data)	Indicates a Data Cycle (can be a Read Data or a Burst Read Data or a Write Data or a Burst Write Data)
(GPCM-Read Cycle)	Indicates a GPCM Read Cycle
(GPCM-Write Cycle)	Indicates a GPCM Write Cycle
(GPCM-Wait Cycle)	Indicates a GPCM Wait Cycle
(No Device Selected for CS0)	Indicates that Chip Select 0 (CS0~) disassembly option is not selecting any device *

Table 2-6: Cycle type label definitions for the 8101_SNG support (cont.)

Cycle type	Definition
(No Device Selected for CS1)	Indicates that Chip Select 1 (CS1~) disassembly option is not selecting any device *
(No Device Selected for CS2)	Indicates that Chip Select 2 (CS2~) disassembly option is not selecting any device *
(No Device Selected for CS3)	Indicates that Chip Select 3 (CS3~) disassembly option is not selecting any device *
(No Device Selected for CS4)	Indicates that Chip Select 4 (CS4~) disassembly option is not selecting any device *
(No Device Selected for CS5)	Indicates that Chip Select 5 (CS5~) disassembly option is not selecting any device *
(No Device Selected for CS6)	Indicates that Chip Select 6 (CS6~) disassembly option is not selecting any device *
(No Device Selected for CS7)	Indicates that Chip Select 7 (CS7~) disassembly option is not selecting any device *

* **The support displays this label when the CSn~ Disassembly option selected is 'No_Device'.**

Table 2-7: Cycle type label definitions for the 8101_MLT support

Cycle type	Definition
(Transfer Start)	Indicates TS~ is asserted
(Transfer Error)	Indicates TEA~ is asserted
(Address)	Indicates a valid Address
(Address Bus Busy)	Indicates ABB~ is asserted
(Address Acknowledge)	Indicates AACK~ is asserted
(Address Retry)	Indicates ARTRY~ is asserted
(Data)	Indicates valid data
(Burst Data)	Indicates TBST~ is asserted for Burst Data
(Data Bus Busy)	Indicates DBB~ is asserted
(Transfer Acknowledge)	Indicates TA~ is asserted
(Bus Grant)	Indicates BG0~ or BG~ or EXT_BG2~ or EXT_BG3~ is asserted
(No Device Selected for CS0)	Indicates that Chip Select 0 (CS0~) disassembly option is not selecting any device *
(No Device Selected for CS1)	Indicates that Chip Select 1 (CS1~) disassembly option is not selecting any device *

Table 2-7: Cycle type label definitions for the 8101_MLT support (cont.)

Cycle type	Definition
(No Device Selected for CS2)	Indicates that Chip Select 2 (CS2~) disassembly option is not selecting any device *
(No Device Selected for CS3)	Indicates that Chip Select 3 (CS3~) disassembly option is not selecting any device *
(No Device Selected for CS4)	Indicates that Chip Select 4 (CS4~) disassembly option is not selecting any device *
(No Device Selected for CS5)	Indicates that Chip Select 5 (CS5~) disassembly option is not selecting any device *
(No Device Selected for CS6)	Indicates that Chip Select 6 (CS6~) disassembly option is not selecting any device *
(No Device Selected for CS7)	Indicates that Chip Select 7 (CS7~) disassembly option is not selecting any device *

* **The support displays this label when the CSn~ Disassembly option selected is 'No_Device'.**

A unique label is attached to the cycle type labels that identifies the cycles corresponding to every processor.

- For the main master (internal arbiter) or processor0 (external arbiter) cycles, the support indicates '-> Processor_0 Cycle'
- For the second processor cycles, the support indicates '-> Processor_1'
- For the third processor cycles, the support indicates '-> Processor_2'
- For the fourth processor cycles, the support indicates '-> Processor_3'

For example: A 'Transfer Start' Cycle of the second processor is labeled as (Transfer Start) -> Processor_1

Table 2–8 shows the general cycle type labels and their descriptions that the support recognizes and displays.

Table 2-8: General cycle type labels

Cycle type	Definition
(Idle Cycle)	Indicates the cycle that is in between two valid cycles
(Unknown Cycle)	Indicates the cycle that is not yet identified and decoded
Un-Associated Data	Indicates that no address is available for associating with a data beat (because of incomplete acquisition of the complete cycle) or when the address is re-tried and data tenure already exists

NOTE**. The label 'Idle Cycle' is common for both supports. The label 'Unknown Cycle' is used in 8101_SNG support and the label ***Un-Associated Data is used in 8101_MLT support.*

Use the Micro Specific Fields in the 8101_MLT support to view the cycle type labels of all the processors simultaneously or of one processor at a time.

Figure 2–4 shows an example of the Hardware Display format in the Single Master Mode.

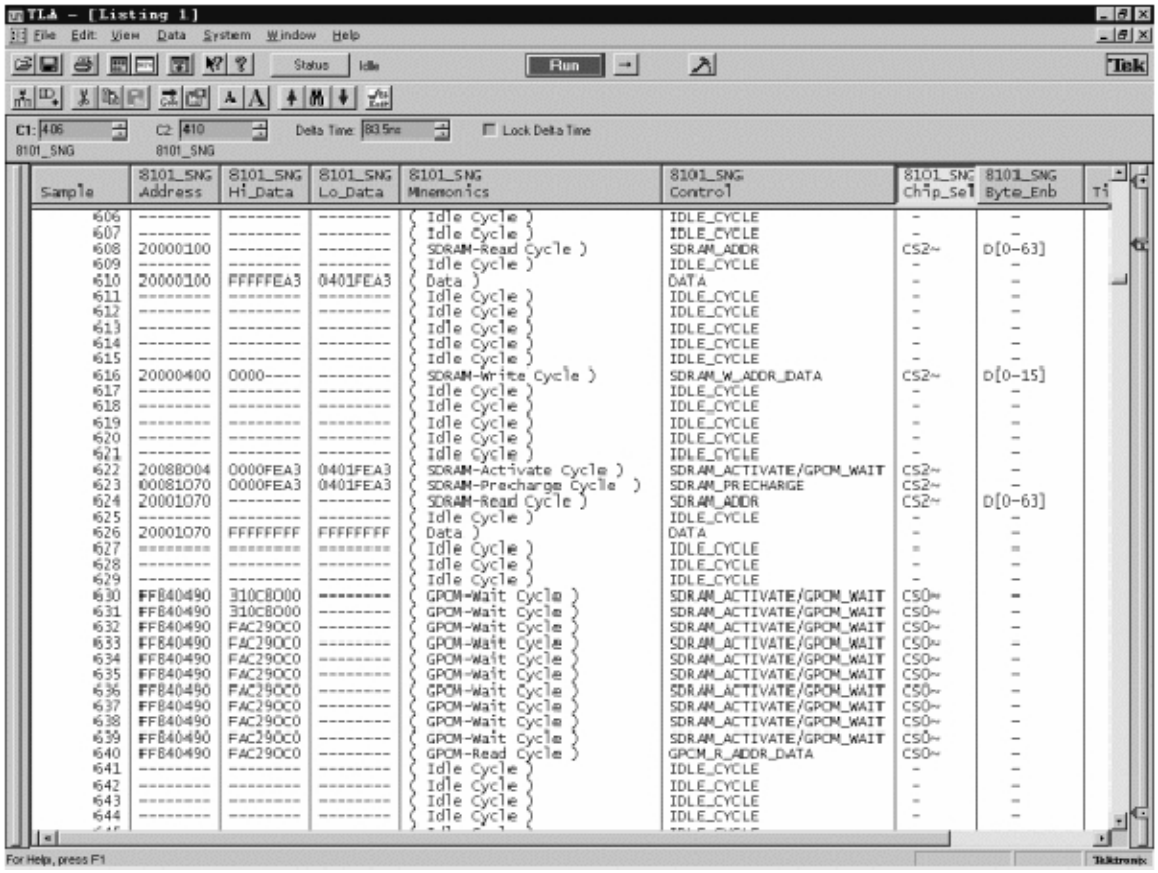


Figure 2–4: Example of the Hardware Display format in the Single Master Mode

Figure 2–5 shows an example of the Hardware Display format in the Multi Master Mode.

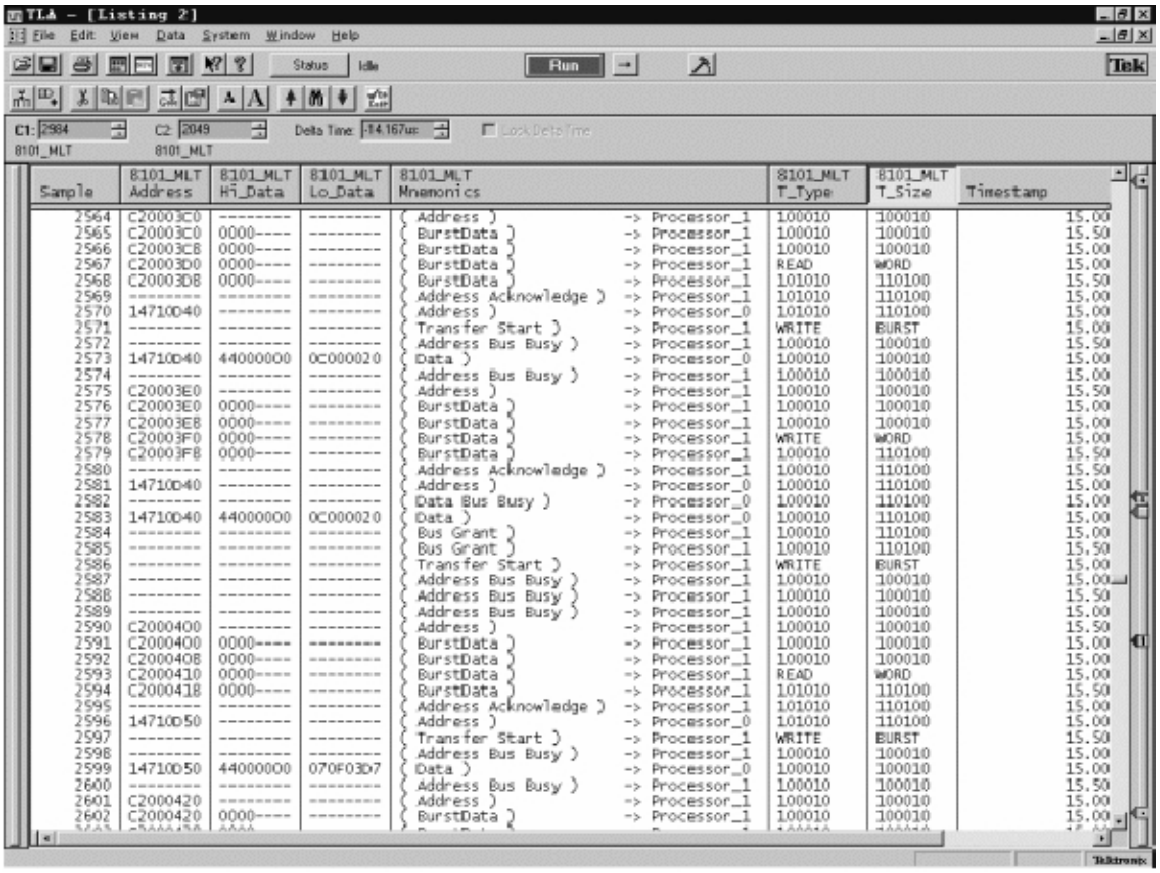


Figure 2–5: Example of the Hardware Display format in the Multi Master Mode

Changing How Labels are Displayed

There are common fields and features that allow you to further modify displayed data to suit your needs. You can make common and optional display selections in the Disassembly property page (the Disassembly Format Definition overlay).

You can make selections unique to the TMS708 support to do the following tasks:

- Change the interpretation of cycle type labels
- Display exception cycles

Optional Display Selections

You can make optional selections for disassembled data. In addition to the common selections (described in the information on basic operations), you can change the displayed data as shown in Table 2-9:

Table 2-9: Logic analyzer disassembly display options

Description	Option	
Show:	Hardware	(Default)
Highlight:	None	
Disassemble Across Gaps:	Yes No	 (Default)

Micro-Specific Fields for 8101_SNG

The following micro-specific fields are available in the Disassembly options page.

This submenu has the title: 8101_SNG Controls. For the 8101_SNG Support package the micro-specific fields are:

Idle Cycles. Use this option to show or suppress the idle cycles in the hardware display format. Select one of the following options:

Idle Cycles: Show (default)
Suppress

CAS Latency. Select the CAS Latency value for correct disassembly. The CAS Latency option represents the CL field of the SDRAM configuration register (PSDMR).

CAS Latency: 1 (default)
2
3

Vector Base Address. Input the base address for the vector table. The vector base address reflects the value set in the VBA register. The vector base address is a five digit field that forms the 20-bit MSB of the vector address.

CS0~. Select the port size and memory device for CS0~ by selecting one of the following options.

CS0~:
- SDRAM-64 Bit (default)
- SDRAM-32 Bit
- SDRAM-16 Bit
- SDRAM-8 Bit
- GPCM-64 Bit
- GPCM-32 Bit
- GPCM-16 Bit
- GPCM-8 Bit
- No_Device

CS1~. Select the port size and memory device for CS1~ by selecting one of the following options.

CS1~:
- SDRAM-64 Bit (default)
- SDRAM-32 Bit
- SDRAM-16 Bit
- SDRAM-8 Bit
- GPCM-64 Bit
- GPCM-32 Bit
- GPCM-16 Bit
- GPCM-8 Bit
- No_Device

CS2~. Select the port size and memory device for CS2~ by selecting one of the following options.

CS2~:
- SDRAM-64 Bit (default)
- SDRAM-32 Bit
- SDRAM-16 Bit
- SDRAM-8 Bit
- GPCM-64 Bit
- GPCM-32 Bit
- GPCM-16 Bit
- GPCM-8 Bit
- No_Device

CS3~. Select the port size and memory device for CS3~ by selecting one of the following options.

CS3~:
- SDRAM-64 Bit (default)
- SDRAM-32 Bit
- SDRAM-16 Bit
- SDRAM-8 Bit
- GPCM-64 Bit
- GPCM-32 Bit
- GPCM-16 Bit
- GPCM-8 Bit
- No_Device

CS4~. Select the port size and memory device for CS4~ by selecting one of the following options.

CS4~:
- SDRAM-64 Bit (default)
- SDRAM-32 Bit
- SDRAM-16 Bit
- SDRAM-8 Bit
- GPCM-64 Bit
- GPCM-32 Bit
- GPCM-16 Bit
- GPCM-8 Bit
- No_Device

CS5~. Select the port size and memory device for CS5~ by selecting one of the following options.

CS5~:
- SDRAM-64 Bit (default)
- SDRAM-32 Bit
- SDRAM-16 Bit
- SDRAM-8 Bit
- GPCM-64 Bit
- GPCM-32 Bit
- GPCM-16 Bit
- GPCM-8 Bit
- No_Device

CS6~. Select the port size and memory device for CS6~ by selecting one of the following options.

CS6~:
- SDRAM-64 Bit (default)
- SDRAM-32 Bit
- SDRAM-16 Bit
- SDRAM-8 Bit
- GPCM-64 Bit
- GPCM-32 Bit
- GPCM-16 Bit
- GPCM-8 Bit
- No_Device

CS7~. Select the port size and memory device for CS7~ by selecting one of the following options.

CS7~:
- SDRAM-64 Bit (default)
- SDRAM-32 Bit
- SDRAM-16 Bit
- SDRAM-8 Bit
- GPCM-64 Bit
- GPCM-32 Bit
- GPCM-16 Bit
- GPCM-8 Bit
- No_Device

Micro-Specific Fields for 8101_MLT

This submenu will have the title: 8101_MLT Controls. For the 8101_MLT Support package the micro-specific fields are:

Idle Cycles. Use the Idle Cycles option to show or suppress the idle cycles in the hardware display format. Select one of the following options:

Idle Cycles:
- Show (default)
- Suppress

Arbiter. Use the Arbiter option to identify the multi-master configuration (Internal or External Arbiter) in the target system. Select one of the following options:

Arbiter:
- Internal (default)
- External

Selecting Internal or External changes the definition of the next option ‘Show Cycles Of’.

Show Cycles Of. You can view either the cycles of any one master at a time, or all the masters by selecting one of the following options.

Show Cycles Of: All (default)
0
1
2
3

NOTE*. When you set the Arbiter option to Internal , the definitions of 0, 1, 2, and 3 are as follows:*

0 represents the MSC8101 main master (or the Internal Arbiter)
1, 2, and 3 represent the other three external masters connected on the same bus
BR~, BG~, DBG~ reflect the status of Main master and Processor 1
BR2~, BG2~, DBG2~ reflect the status of Processor 2
BR3~, BG3~, DBG3~ reflect the status of Processor 3

When you set the Arbiter option to External, the definitions of 0, 1, 2, and 3 are as follows:

1, 2, 3, and 4 represent the four external masters connected to the bus
TC0/BR0~, TC1/BG0~, TC2/DBG0~ reflects the status of Processor 0
BR~, BG~, DBG~ reflect the status of Processor 1
BR2~, BG2~, DBG2~ reflect the status of Processor 2
BR3~, BG3~, DBG3~ reflect the status of Processor 3

Signals Connected Are. For burst transactions in the multi master mode, address increments are visible if signals BADDR[31-27] are connected to logic analyzer channels A0[0-4]. If signals A[31–27] are connected to logic analyzer channels A0[0-4], the software performs the address increments. Select one of the following options.

Signals Connected Are: A[27–31] (default)
BADDR[27–31]

Vector Base Address. Input the base address for the vector table. The vector base address reflects the value set in the VBA register. The vector base address is a five digit field that forms the 20-bit MSB of the vector address.

CS0~. Select the port size for CS0~ by selecting one of the following options.

CS0~: 64 Bit (default)
32 Bit
16 Bit
8 Bit
No_Device

CS1~. Select the port size for CS1~ by selecting one of the following options.

CS1~: 64 Bit (default)
32 Bit
16 Bit
8 Bit
No_Device

CS2~. Select the port size for CS2~ by selecting one of the following options.

CS2~: 64 Bit (default)
32 Bit
16 Bit
8 Bit
No_Device

CS3~. Select the port size for CS3~ by selecting one of the following options.

CS3~: 64 Bit (default)
32 Bit
16 Bit
8 Bit
No_Device

CS4~. Select the port size for CS4~ by selecting one of the following options.

CS4~: 64 Bit (default)
32 Bit
16 Bit
8 Bit
No_Device

CS5~. Select the port size for CS5~ by selecting one of the following options.

CS5~:
- 64 Bit (default)
- 32 Bit
- 16 Bit
- 8 Bit
- No_Device

CS6~. Select the port size for CS6~ by selecting one of the following options.

CS6~:
- 64 Bit (default)
- 32 Bit
- 16 Bit
- 8 Bit
- No_Device

CS7~. Select the port size for CS7~ by selecting one of the following options.

CS7~:
- 64 Bit (default)
- 32 Bit
- 16 Bit
- 8 Bit
- No_Device

Marking Cycles

The support has a Mark Opcode function that allows you to change the interpretation of a cycle type. Using this function, you can select a cycle and change it.

Marks are placed by using the Mark Opcode button. The Mark Opcode button is always available. If the sample being marked is not a Data cycle in 8101_MLT or an Address cycle in 8101_SNG of the potential bus master, the Mark Opcode selections are replaced by a note indicating that 'An Opcode Mark cannot be placed at the selected data sample.'

When a cycle is marked, the character '>>' is displayed immediately to the left of the Mnemonics column. Cycles can be unmarked by using the 'Undo Mark' selection, which removes the character '>>'. Tables 2–10 and 2–11 show the mark selections and definitions for the Single and Multi Master support.

The mark selections listed in Table 2–10 are available only for address sequences.

Table 2–10: Mark selections and definitions for 8101_SNG support

Mark selections	Definition
Read -> Fetch	Read can be marked as Fetch
Undo Mark	Removes all marks from the current sequence

The mark selections listed in Table 2–11 are available only for data sequences.

Table 2–11: Mark selections and definitions for 8101_MLT support

Mark selections	Definition
Invalid Data	Any of the Data Cycles can be marked as Invalid Data bits. No address is associated for this data.
Undo Mark	Removes all marks from the current sequence

Displaying Exception Labels

The support can display MSC8101 exception labels. The exception table must reside in external memory for interrupt and exception cycles to be visible to the disassembler.

You can enter the table prefix in the Vector Base Address field. The Vector Base Address field provides the support with the address. Enter a 5-digit hexadecimal value corresponding to the prefix of the exception table.

These fields are located in the Disassembly property page (Disassembly Format Definition overlay).

Table 2–12 lists the MSC8101 interrupt and exception labels.

Table 2–12: Interrupt and exception labels

Offset in hex	Displayed interrupt or exception name
000	(Internal (TRAP) Exception)
040	(Reserved Exception)
080	(Illegal Instruction or Set Exception)
0C0	(Debug (EOnCE) Exception)
100	(Reserved Exception)
140	(Overflow (DALU) Exception)
180	(Auto-NMI Exception)
1C0	(Auto-IRQ Exception)

Table 2-12: Interrupt and exception labels (cont.)

Offset in hex	Displayed interrupt or exception name
200-7C0	(Reserved Exception)
800	(EFCOP(0):Input FIFO Not Full Exception)
840	(EFCOP(1):Input FIFO Empty Exception)
880	(EFCOP(2):Output FIFO Full Exception)
8C0	(EFCOP(3):Output FIFO Not Empty Exception)
900	(EFCOP(4):Update Done Exception)
940	(HDI16(0):Receive FIFO Full Exception)
980	(HDI16(1):Receive FIFO Not Empty Exception)
9C0	(HDI16(2):Transmit FIFO Empty Exception)
A00	(HDI16(3):Transmit FIFO Not Full Exception)
A40	(HDI16(4):External HOST Command Exception)
A80	(Bus Controller (x-y contention) Exception)
AC0	(Bus Controller (Level 1 Contention) Exception)
B00	(Bus Controller (p-x Contention) Exception)
B40	(Bus Controller (Non-Aligned Data Error) Exception)
B80	(PIC Interrupt Request)
BC0	(External IRQ2 Exception)
C00	(SIC Interrupt)
C40	(External IRQ3 Interrupt)
C80	(DMA Interrupt)
CC0	(Reserved Exception)
D00	(EOnCE Interrupt)
D40-DC0	(Reserved Exception)
E00	(HDI16:External HOST NMI Interrupt)
E40	(Reserved Exception)
E80	(Bus Controller (Memory Write Error) Exception)
EC0	(Bus Controller (Non-Aligned Error) Exception)
F00	(Bus Controller (Bus Error) Exception)
F40-F80	(Reserved Exception)
FC0	(SIC NMI Exception)

Viewing an Example of Cycle Type Labels

A demonstration system file (or demonstration reference memory) for the support package is provided on your software disk to show an example of how your MSC8101 microprocessor bus cycles look when they are decoded. Viewing the system file is not a requirement for preparing the module for use and you can view it without connecting the logic analyzer to your target system.

Information on basic operations describes how to view the file.

Reference

Reference: Symbol and Channel Assignment Tables

This section lists the symbol tables and channel assignment tables for disassembly and timing.

Symbol Tables

The TMS708 support supplies nine symbol-table files. In the 8101_SNG support, the 8101_SNG_Control file replaces specific Control group values with symbolic values. In the 8101_MLT support, the 8101_MLT_Control file replaces specific Control group values with symbolic values. Symbol files can be applied to a group when the radix Symbolic is chosen.

Symbol tables are generally not for use in timing or MSC8101_T support cycle type decoding.

8101_SNG Support

Tables 3–1 through 3–3 show the definitions for name, bit pattern, and meaning of the group symbols in the files 8101_SNG_Control, 8101_SNG_Chip_Sel, and 8101_SNG_Byte_Enb for 8101_SNG support.

Table 3-1: 8101_SNG_Control group symbol table definitions

Symbol	Control group value HRESET~ SRESET~ PORESET~ PSDRAS~/POE~~ PSDCAS~ PSDVAL~ PSDWE~ PSDAMUX PSDA10 PGTA~ BCTL1~ BCTL0~ GBL~	Description
SDRAM_PRECHARGE	1 1 1 0 1 X 0 X X X X X X	#SDRAM Precharge Command
SDRAM_ACTIVATE/ GPCM_WAIT	1 1 1 0 1 1 1 X X X X X X	#SDRAM Activate Command or GPCM Wait Cycle
SDRAM_REFRESH	1 1 1 0 0 X 1 X X X X X X	#SDRAM Refresh Command
SDRAM_W_ADDR_DATA	1 1 1 1 0 0 0 X X X X X X	#SDRAM Write Address + Data Cycle
SDRAM_R_ADDR_DATA	1 1 1 1 0 0 1 X X X X X X	#SDRAM Read Address Cycle + Data for previous transaction
SDRAM_ADDR	1 1 1 1 0 1 1 X X X X X X	#SDRAM Read Address Cycle
GPCM_R_ADDR_DATA	1 1 1 0 1 0 1 X X X X X X	#GPCM Read Address + Data Cycle
GPCM_W_ADDR_DATA	1 1 1 1 1 0 0 X X X X X X	#GPCM Write Address + Data Cycle

Table 3-1: 8101_SNG_Control group symbol table definitions (cont.)

Symbol	Control group value HRESET~ SRESET~ PORESET~ PSDRAS~/POE~~ PSDCAS~ PSDVAL~ PSDWE~ PSDAMUX PSDA10 PGTA~ BCTL1~ BCTL0~ GBL~	Description
SDRAM_ROW_ADDR	1 1 1 0 X X X X X X X X X	#SDRAM Row Address
SDRAM_COL_ADDR	1 1 1 X 0 X X X X X X X X	#SDRAM Column Address
DATA	1 1 1 X X 0 X X X X X X X	#Data Cycle
IDLE_CYCLE	1 1 1 1 1 1 X X X X X X X	#Idle Cycle (SDRAM CAS Latency or GPCM Wait State)
HRESET	0 X X X X X X X X X X X X	#Hardware Reset Cycle
SRESET	X 0 X X X X X X X X X X X	#Software Reset Cycle
PORESET	X X 0 X X X X X X X X X X	#Power On Reset Cycle

Table 3-2: 8101_SNG_Chip_Sel group symbol table definitions

Symbol	Chip_Sel group value CS0~ CS1~ CS2~ CS3~ CS4~ CS5~ CS6~ CS7~	Description
CS0~	0 1 1 1 1 1 1 1	#Device 0 Selected
CS1~	1 0 1 1 1 1 1 1	#Device 1 Selected
CS2~	1 1 0 1 1 1 1 1	#Device 2 Selected
CS3~	1 1 1 0 1 1 1 1	#Device 3 Selected
CS4~	1 1 1 1 0 1 1 1	#Device 4 Selected
CS5~	1 1 1 1 1 0 1 1	#Device 5 Selected
CS6~	1 1 1 1 1 1 0 1	#Device 6 Selected
CS7~	1 1 1 1 1 1 1 0	#Device 7 Selected
-	1 1 1 1 1 1 1 1	#No Devices Selected

Table 3-3: 8101_SNG_Byte_Enb group symbol table definitions

Symbol	Byte_Enb group value PWE0~ PWE1~ PWE2~ PWE3~ PWE4~ PWE5~ PWE6~ PWE7~	Description
D [0-7]	0 1 1 1 1 1 1 1	#Byte Lane 0 Selected
D [8-15]	1 0 1 1 1 1 1 1	#Byte Lane 1 Selected

Table 3-3: 8101_SNG_Byte_Enb group symbol table definitions (cont.)

Symbol	Byte_Enb group value PWE0~ PWE1~ PWE2~ PWE3~ PWE4~ PWE5~ PWE6~ PWE7~	Description
D [16-23]	1 1 0 1 1 1 1 1	#Byte Lane 2 Selected
D [24-31]	1 1 1 0 1 1 1 1	#Byte Lane 3 Selected
D [32-39]	1 1 1 1 0 1 1 1	#Byte Lane 4 Selected
D [40-47]	1 1 1 1 1 0 1 1	#Byte Lane 5 Selected
D [48-55]	1 1 1 1 1 1 0 1	#Byte Lane 6 Selected
D [56-63]	1 1 1 1 1 1 1 0	#Byte Lane 7 Selected
D [0-15]	0 0 1 1 1 1 1 1	#Byte Lane 0-1 Selected
D [8-23]	1 0 0 1 1 1 1 1	#Byte Lane 1-2 Selected
D [16-31]	1 1 0 0 1 1 1 1	#Byte Lane 2-3 Selected
D [32-47]	1 1 1 1 0 0 1 1	#Byte Lane 4-5 Selected
D [40-55]	1 1 1 1 1 0 0 1	#Byte Lane 5-6 Selected
D [48-63]	1 1 1 1 1 1 0 0	#Byte Lane 6-7 Selected
D [0-23]	0 0 0 1 1 1 1 1	#Byte Lane 0-1-2 Selected
D [8-31]	1 0 0 0 1 1 1 1	#Byte Lane 1-2-3 Selected
D [32-55]	1 1 1 1 0 0 0 1	#Byte Lane 4-5-6 Selected
D [40-63]	1 1 1 1 1 0 0 0	#Byte Lane 5-6-7 Selected
D [0-31]	0 0 0 0 1 1 1 1	#Byte Lane 0-1-2-3 Selected
D [32-63]	1 1 1 1 0 0 0 0	#Byte Lane 4-5-6-7 Selected
D [0-63]	0 0 0 0 0 0 0 0	#All Byte Lanes Selected
-	1 1 1 1 1 1 1 1	#No Byte Lanes Selected

Information on basic operations describes how to use symbolic values for triggering and for displaying other channel groups symbolically, such as for the Address channel group.

8101_MLT Support

Tables 3-4 through 3-9 show the definitions for name, bit pattern, and meaning of the group symbols in the files 8101_MLT_Control, 8101_MLT_Chip_Sel, 8101_MLT_T_Type, 8101_MLT_T_Size, 8101_MLT_T_Code, and 8101_MLT_Req_Grant for 8101_MLT support.

Table 3-4: 8101_MLT_Control group symbol table definitions

Symbol	Control group value TS~ ALE ABB~ AACK~ PSDVAL~ DBB~ TA~ TEA~ ARTRY~	Description
TRANSFER_ERROR	X X X X X X X 0 X	#Transfer Error Cycle
TRANSFER_START	0 X X X 1 X 1 X X	#Transfer Start Cycle
ADDRESS_RETRY	X X X X X X X X 0	#Address Retry Cycle
DATA	X X X X 0 X X X X	#Data
ADDRESS_LATCH	X 1 X X X X X X X	#Address Latch Cycle
ADDRESS_ACK.	X X X 0 X X X X X	#Address Acknowledge Cycle
TRANSFER_ACK.	X X X X X X 0 X X	#Transfer Acknowledge Cycle
ADDR._BUS_BUSY	X X 0 X X X X X X	#Address Bus Busy Cycle
DATA_BUS_BUSY	X X X X X 0 X X X	#Data Bus Busy Cycle

Table 3-5: 8101_MLT_Chip_Sel group symbol table definitions

Symbol	Chip_Sel group value CS0~ CS1~ CS2~ CS3~ CS4~ CS5~ CS6~ CS7~	Description
CS0~	0 1 1 1 1 1 1 1	#Device 0 Selected
CS1~	1 0 1 1 1 1 1 1	#Device 1 Selected
CS2~	1 1 0 1 1 1 1 1	#Device 2 Selected
CS3~	1 1 1 0 1 1 1 1	#Device 3 Selected
CS4~	1 1 1 1 0 1 1 1	#Device 4 Selected
CS5~	1 1 1 1 1 0 1 1	#Device 5 Selected
CS6~	1 1 1 1 1 1 0 1	#Device 6 Selected
CS7~	1 1 1 1 1 1 1 0	#Device 7 Selected
-	1 1 1 1 1 1 1 1	#No Devices Selected

Table 3-6: 8101_MLT_T_Type group symbol table definitions

Symbol	T_Type group value TS~ TT0 TT1 TT2 TT3 TT4	Description
RESERVED	0 0 0 1 0 1	Reserved
RESERVED_FOR_CUSTOMER	0 1 X X 0 1	Reserved for Customer
WRITE	0 0 0 0 1 0	Write Transaction (Single Beat or Burst)
READ	0 0 1 0 1 0	Read Transaction (Single Beat or Burst)
RESERVED	0 1 0 1 1 0	Reserved
RESERVED	0 0 0 0 1 1	Reserved
RESERVED	0 0 0 1 1 1	Reserved
RESERVED	0 0 1 1 1 1	Reserved
RESERVED_FOR_CUSTOMER	0 1 X X 1 1	Reserved for Customer

Table 3-7: 8101_MLT_T_Size group symbol table definitions

Symbol	T_Size group value TS~ TBST~ TSIZ0 TSIZ1 TSIZ2 TSIZ3	Description
BYTE	0 1 0 0 0 1	1 Byte Transaction
HALF_WORD	0 1 0 0 1 0	2 Bytes Transaction
TRIPLE_BYTE	0 1 0 0 1 1	3 Bytes Transaction
WORD	0 1 0 1 0 0	4 Bytes Transaction
EXTENDED_5_BYTES	0 1 0 1 0 1	Extended 5 Bytes Transaction
EXTENDED_6_BYTES	0 1 0 1 1 0	Extended 6 Bytes Transaction
EXTENDED_7_BYTES	0 1 0 1 1 1	Extended 7 Bytes Transaction
DOUBLE_WORD	0 1 0 0 0 0	8 Bytes Transaction
BURST	0 0 X X X X	Burst Transaction

Table 3-8: 8101_MLT_T_Code group symbol table definitions

Symbol	T_Code group value TS~ TC0/BR0~ TC1/BG0~ TC2/DBG0~	Description
RESERVED	0 0 0 0	Reserved
RESERVED	0 0 0 1	Reserved
RESERVED	0 0 1 0	Reserved
RESERVED	0 0 1 1	Reserved
DMA	0 1 0 0	DMA Source
SC140_CORE/DMA	0 1 0 1	SC140 or DMA Source
SDMA_FUNCTION_CODE_0	0 1 1 0	SDMA Function Code 0 Source
SDMA_FUNCTION_CODE_1	0 1 1 1	SDMA Function Code 1 Source

***NOTE**. The T_Code group is applicable only in Internal Arbiter Mode.*

Table 3-9: 8101_MLT_Req_Grant group symbol table definitions

Symbol	Req_Grant group value TCO/BR0~ TC1/BG0~ TC2/DBG0~ BR~ BG~ DBG~ DP0~/EXT_BR2~ DP1/EXT_BG2~ DP2~/EXT_DBG2~ DP3~/EXT_BR3~ DP4~/EXT_BG3~ DP5~/EXT_DBG3~	Description
BG0_ADDRESS	X X X X 0 1 1 1 1 1 1 1	#BG0~ Asserted
BG_ADDRESS	X X X X 1 0 1 1 1 1 1 1	#BG~ Asserted
BG2_ADDRESS	X X X X 1 1 0 1 1 1 1 1	#BG2~ Asserted
BG3_ADDRESS	X X X X 1 1 1 0 1 1 1 1	#BG3~ Asserted
DBG0_DATA	X X X X 1 1 1 1 0 1 1 1	#DBG0~ Asserted
DBG_DATA	X X X X 1 1 1 1 1 0 1 1	#DBG~ Asserted
DBG2_DATA	X X X X 1 1 1 1 1 1 0 1	#DBG2~ Asserted
DBG3_DATA	X X X X 1 1 1 1 1 1 1 0	#DBG3~ Asserted

Channel Assignment Tables

Channel assignments shown in Tables 3–10 through 3–25 use the following conventions:

- All signals are required by the support unless indicated otherwise.
- Channels are shown starting with the most significant bit (MSB) descending to the least significant bit (LSB).
- Channel group assignments are for all modules unless otherwise noted.
- A tilde (~) following a signal name indicates an active low signal.

8101_SNG Support

Table 3–10 shows the probe section and channel assignments for the logic analyzer Address group and the microprocessor signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3-10: Address group channel assignments for 8101_SNG support

Bit order	MSC8101 signal name
A3:7 (MSB)	A0
A3:6	A1
A3:5	A2
A3:4	A3
A3:3	A4
A3:2	A5
A3:1	A6
A3:0	A7
A2:7	A8
A2:6	A9
A2:5	A10
A2:4	A11
A2:3	A12
A2:2	A13
A2:1	A14
A2:0	A15
A1:7	A16
A1:6	A17
A1:5	A18

Table 3-10: Address group channel assignments for 8101_SNG support (cont.)

Bit order	MSC8101 signal name
A1:4	A19
A1:3	A20
A1:2	A21
A1:1	A22
A1:0	A23
A0:7	A24
A0:6	A25
A0:5	A26
A0:4	A27
A0:3	A28
A0:2	A29
A0:1	A30
A0:0 (LSB)	A31

Table 3–11 shows the probe section and channel assignments for the Hi_Data group and the microprocessor signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3-11: Hi_Data group channel assignments for 8101_SNG support

Bit order	MSC8101 signal name
E3:7 (MSB)	D0
E3:6	D1
E3:5	D2
E3:4	D3
E3:3	D4
E3:2	D5
E3:1	D6
E3:0	D7
E2:7	D8
E2:6	D9
E2:5	D10
E2:4	D11

Table 3-11: Hi_Data group channel assignments for 8101_SNG support (cont.)

Bit order	MSC8101 signal name
E2:3	D12
E2:2	D13
E2:1	D14
E2:0	D15
E1:7	D16
E1:6	D17
E1:5	D18
E1:4	D19
E1:3	D20
E1:2	D21
E1:1	D22
E1:0	D23
E0:7	D24
E0:6	D25
E0:5	D26
E0:4	D27
E0:3	D28
E0:2	D29
E0:1	D30
E0:0	D31

Table 3–12 shows the probe section and channel assignments for the Lo_Data group and the microprocessor signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3-12: Lo_Data group channel assignments for 8101_SNG support

Bit order	MSC8101 signal name
D3:7	D32
D3:6	D33
D3:5	D34
D3:4	D35
D3:3	D36

Table 3-12: Lo_Data group channel assignments for 8101_SNG support (cont.)

Bit order	MSC8101 signal name
D3:2	D37
D3:1	D38
D3:0	D39
D2:7	D40
D2:6	D41
D2:5	D42
D2:4	D43
D2:3	D44
D2:2	D45
D2:1	D46
D2:0	D47
D1:7	D48
D1:6	D49
D1:5	D50
D1:4	D51
D1:3	D52
D1:2	D53
D1:1	D54
D1:0	D55
D0:7	D56
D0:6	D57
D0:5	D58
D0:4	D59
D0:3	D60
D0:2	D61
D0:1	D62
D0:0 (LSB)	D63

Table 3–13 shows the probe section and channel assignments for the Control group and the microprocessor signal to which each channel connects. By default, this channel group is displayed as symbols.

Table 3-13: Control group channel assignments for 8101_SNG support

Bit order	MSC8101 signal name
C1:1	HRESET~
C1:0	SRESET~
C0:6	PORESET~
C0:1	PSDRAS~/POE~
CLK:3	PSDCAS~
CLK:0	PSDVAL~
C1:7	PSDWE~
C1:4	PSDAMUX
C1:6	PSDA10
C1:5	PGTA~
C0:2	BCTL1~
C1:3	BCTL0~
C0:7	GBL~

Table 3–14 shows the probe section and channel assignments for the Chip_Sel group and the microprocessor signal to which each channel connects. By default, this channel group is displayed as symbols.

Table 3-14: Chip_Sel group channel assignments for 8101_SNG support

Bit order	MSC8101 signal name
QUAL:3	CS0~
QUAL:2	CS1~
QUAL:0	CS2~
CLK:2	CS3~
C2:7	CS4~
C2:6	CS5~
C2:5	CS6~
C2:4	CS7~

Table 3–15 shows the probe section and channel assignments for the Byte_Enb group and the microprocessor signal to which each channel connects. By default, this channel group is displayed as binary.

Table 3-15: Byte_Enb group channel assignments for 8101_SNG support

Bit order	MSC8101 signal name
C3:7	PWE0~
C3:6	PWE1~
C3:5	PWE2~
C3:4	PWE3~
C3:3	PWE4~
C3:2	PWE5~
C3:1	PWE6~
C3:0	PWE7~

Table 3–16 shows the probe section and channel assignments for the logic analyzer Misc group and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3-16: Misc group channel assignments for 8101_SNG support

Bit order	MSC8101 signal name
CLK:1	CLKOUT
C0:5	NMI~
C1:2	NMI_OUT~
QUAL:1	IRQ7~/INT_OUT~
C0:4	DP6~/EXT_DACK3~
C0:3	DP7~/EXT_DACK4~

8101_MLT Support

Table 3–17 shows the probe section and channel assignments for the logic analyzer Address group and the microprocessor signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3- 17: Address group channel assignments for 8101_MLT support

Bit order	MSC8101 signal name
A3:7 (MSB)	A0
A3:6	A1
A3:5	A2
A3:4	A3
A3:3	A4
A3:2	A5
A3:1	A6
A3:0	A7
A2:7	A8
A2:6	A9
A2:5	A10
A2:4	A11
A2:3	A12
A2:2	A13
A2:1	A14
A2:0	A15
A1:7	A16
A1:6	A17
A1:5	A18
A1:4	A19
A1:3	A20
A1:2	A21
A1:1	A22
A1:0	A23
A0:7	A24
A0:6	A25
A0:5	A26
A0:4	BADDR27/A27*
A0:3	BADDR28/A28*

Table 3-17: Address group channel assignments for 8101_MLT support (cont.)

Bit order	MSC8101 signal name
A0:2	BADDR29/A29*
A0:1	BADDR30/A30*
A0:0 (LSB)	BADDR31/A31*

* **You can trigger on Burst Address increments only if BADDR[31-27] is connected to logic analyzer channels A0:[0-4]. For more details, refer to *Triggering on Address in a Burst Transaction* on page 1-2.**

Table 3–18 shows the probe section and channel assignments for the Hi_Data group and the microprocessor signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3-18: Hi_Data group channel assignments for 8101_MLT support

Bit order	MSC8101 signal name
E3:7 (MSB)	D0
E3:6	D1
E3:5	D2
E3:4	D3
E3:3	D4
E3:2	D5
E3:1	D6
E3:0	D7
E2:7	D8
E2:6	D9
E2:5	D10
E2:4	D11
E2:3	D12
E2:2	D13
E2:1	D14
E2:0	D15
E1:7	D16
E1:6	D17
E1:5	D18

Table 3-18: Hi_Data group channel assignments for 8101_MLT support (cont.)

Bit order	MSC8101 signal name
E1:4	D19
E1:3	D20
E1:2	D21
E1:1	D22
E1:0	D23
E0:7	D24
E0:6	D25
E0:5	D26
E0:4	D27
E0:3	D28
E0:2	D29
E0:1	D30
E0:0	D31

Table 3–19 shows the probe section and channel assignments for the Lo_Data group and the microprocessor signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3-19: Lo_Data group channel assignments for 8101_MLT support

Bit order	MSC8101 signal name
D3:7	D32
D3:6	D33
D3:5	D34
D3:4	D35
D3:3	D36
D3:2	D37
D3:1	D38
D3:0	D39
D2:7	D40
D2:6	D41
D2:5	D42
D2:4	D43

Table 3-19: Lo_Data group channel assignments for 8101_MLT support (cont.)

Bit order	MSC8101 signal name
D2:3	D44
D2:2	D45
D2:1	D46
D2:0	D47
D1:7	D48
D1:6	D49
D1:5	D50
D1:4	D51
D1:3	D52
D1:2	D53
D1:1	D54
D1:0	D55
D0:7	D56
D0:6	D57
D0:5	D58
D0:4	D59
D0:3	D60
D0:2	D61
D0:1	D62
D0:0 (LSB)	D63

Table 3–20 shows the probe section and channel assignments for the Control group and the microprocessor signal to which each channel connects. By default, this channel group is displayed as symbols.

Table 3-20: Control group channel assignments for 8101_MLT support

Bit order	MSC8101 signal name
CLK:3	TS~
C3:1	ALE
C3:6	ABB~
QUAL:1	AACK~

Table 3-20: Control group channel assignments for 8101_MLT support (cont.)

Bit order	MSC8101 signal name
CLK:0	PSDVAL~
C2:7	DBB~
C0:3	TA~
C0:2	TEA~
C1:6	ARTRY~

Table 3–21 shows the probe section and channel assignments for the Chip_Sel group and the microprocessor signal to which each channel connects. By default, this channel group is displayed as symbols.

Table 3-21: Chip_Sel group channel assignments for 8101_MLT support

Bit order	MSC8101 signal name
QUAL:3	CS0~
QUAL:2	CS1~
QUAL:0	CS2~
CLK:2	CS3~
C3:7	CS4~
C3:3	CS5~
C2:4	CS6~
C2:3	CS7~

Table 3–22 shows the probe section and channel assignments for the T_Type group and the microprocessor signal to which each channel connects. By default, this channel group is displayed as symbols.

Table 3-22: T_Type group channel assignments for 8101_MLT support

Bit order	MSC8101 signal name
CLK:3	TS~
C1:0	TT0
C0:7	TT1

Table 3-22: T_Type group channel assignments for 8101_MLT support (cont.)

Bit order	MSC8101 signal name
C0:6	TT2
C0:5	TT3
C0:4	TT4

Table 3–23 shows the probe section and channel assignments for the T_Size group and the microprocessor signal to which each channel connects. By default, this channel group is displayed as symbols.

Table 3-23: T_Size group channel assignments for 8101_MLT support

Bit order	MSC8101 signal name
CLK:3	TS~
C1:7	TBST~
C1:4	TSIZ0
C1:3	TSIZ1
C1:2	TSIZ2
C1:1	TSIZ3

Table 3–24 shows the probe section and channel assignments for the T_Code group and the microprocessor signal to which each channel connects. By default, this channel group is displayed as symbols.

Table 3-24: T_Code group channel assignments for 8101_MLT support

Bit order	MSC8101 signal name
CLK:3	TS~
C0:1	TC0/BR0~
C0:0	TC1/BG0~
C2:6	TC2/DBG0~

***NOTE**. The T_Code group is applicable only in Internal Arbiter Mode. For more details refer to* T_Code Group in 8101_MLT Group *on page 1-2.*

Table 3-25 shows the probe section and channel assignments for the Req_Grant group and the microprocessor signal to which each channel connects. By default, this channel group is displayed as symbols.

Table 3-25: Req_Grant group channel assignments for 8101_MLT support

Bit order	MSC8101 signal name
C0:1	TC0/BR0~*
C3:2	BR~
C3:4	DP0~/EXT_BR2~
C2:5	DP3~/EXT_BR3~
C0:0	TC1/BG0~*
C3:5	BG~
C2:2	DP1~/EXT_BG2~
C2:0	DP4~/EXT_BG3~
C2:6	TC2/DBG0~*
C3:0	DBG~
C2:1	DP2~/EXT_DBG2~
C1:5	DP5~/EXT_DBG3~

* **When you use the 8101_MLT support for Internal Arbiter configuration, connect the signals TC0-TC2 to C0:1, C0:0, and C2:6. For External Arbiter configuration, connect the signals BR0~, BG0~, and DBG0~ (request and grant signals from the fourth external master that is connected to the bus) to C0:1, C0:0, and C2:6.**

CPU To Mictor Connections

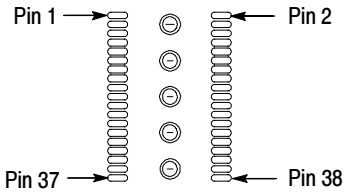
This section contains information about Mictor connections.

For design purposes, you may need to make connections between the CPU and the Mictor pins of the P6434 Mass Termination Probe. Refer to the *P6434 Mass Termination Probe* manual, Tektronix part number 070-9793-XX, for more information on mechanical specifications.

***NOTE**. To preserve signal quality in the target system, you should connect a 180 Ω resistor in series between each ball pad of the CPU and each pin of the Mictor connector. The resistor must be within 1/2 inch of the ball pad of the CPU.*

The recommended pin assignment is the AMP pin assignment, because the AMP circuit board layout model and other commercial CAD packages use the AMP numbering scheme. See Table 3–26.

Table 3-26: Recommended pin assignments for a Mictor connector (component side)

Type of pin assignment	Comments
Recommended  **AMP Pin Assignment**	Recommended. This pin assignment is the industry standard and is what we recommend that you use.

8101_SNG Support

Tables 3–27 through 3–30 show the mictor pin connections for the logic analyzer and the AMP mictors for the 8101_SNG support.

Table 3-27: CPU to Mictor connections for Mictor A pins for 8101_SNG support

AMP mictor pin number	Logic analyzer acquisition channel	MSC8101 support package channel name	Required/Not required for disassembly
Mictor A pin 05	CLOCK:0	PSDVAL~	Required
Mictor A pin 07	A3:7	A0 (MSB)	Required
Mictor A pin 09	A3:6	A1	Required
Mictor A pin 11	A3:5	A2	Required
Mictor A pin 13	A3:4	A3	Required
Mictor A pin 15	A3:3	A4	Required
Mictor A pin 17	A3:2	A5	Required
Mictor A pin 19	A3:1	A6	Required
Mictor A pin 21	A3:0	A7	Required
Mictor A pin 23	A2:7	A8	Required
Mictor A pin 25	A2:6	A9	Required
Mictor A pin 27	A2:5	A10	Required
Mictor A pin 29	A2:4	A11	Required
Mictor A pin 31	A2:3	A12	Required
Mictor A pin 33	A2:2	A13	Required
Mictor A pin 35	A2:1	A14	Required
Mictor A pin 37	A2:0	A15	Required
Mictor A pin 38	A0:0	A31	Required
Mictor A pin 36	A0:1	A30	Required
Mictor A pin 34	A0:2	A29	Required
Mictor A pin 32	A0:3	A28	Required
Mictor A pin 30	A0:4	A27	Required
Mictor A pin 28	A0:5	A26	Required
Mictor A pin 26	A0:6	A25	Required
Mictor A pin 24	A0:7	A24	Required
Mictor A pin 22	A1:0	A23	Required
Mictor A pin 20	A1:1	A22	Required
Mictor A pin 18	A1:2	A21	Required
Mictor A pin 16	A1:3	A20	Required
Mictor A pin 14	A1:4	A19	Required
Mictor A pin 12	A1:5	A18	Required

Table 3-27: CPU to Mictor connections for Mictor A pins for 8101_SNG support (cont.)

AMP mictor pin number	Logic analyzer acquisition channel	MSC8101 support package channel name	Required/Not required for disassembly
Mictor A pin 10	A1:6	A17	Required
Mictor A pin 08	A1:7	A16	Required
Mictor A pin 06	CLOCK:1	CLKOUT	Required

Table 3-28: CPU to Mictor connections for Mictor C pins for 8101_SNG support

AMP mictor pin number	Logic analyzer acquisition channel	MSC8101 support package channel name	Required/Not required for disassembly
Mictor C pin 05	CLOCK:3	PSDCAS~	Required
Mictor C pin 07	C3:7	PWE0~	Required
Mictor C pin 09	C3:6	PWE1~	Required
Mictor C pin 11	C3:5	PWE2~	Required
Mictor C pin 13	C3:4	PWE3~	Required
Mictor C pin 15	C3:3	PWE4~	Required
Mictor C pin 17	C3:2	PWE5~	Required
Mictor C pin 19	C3:1	PWE6~	Required
Mictor C pin 21	C3:0	PWE7~	Required
Mictor C pin 23	C2:7	CS4~	Required
Mictor C pin 25	C2:6	CS5~	Required
Mictor C pin 27	C2:5	CS6~	Required
Mictor C pin 29	C2:4	CS7~	Required
Mictor C pin 31	C2:3	No connection	Not required
Mictor C pin 33	C2:2	No connection	Not required
Mictor C pin 35	C2:1	No connection	Not required
Mictor C pin 37	C2:0	No connection	Not required
Mictor C pin 38	C0:0	No connection	Not required
Mictor C pin 36	C0:1	PSDRAS~/POE~	Required
Mictor C pin 34	C0:2	BCTL1~	Not required
Mictor C pin 32	C0:3	DP7~/DACK4~	Not required
Mictor C pin 30	C0:4	DP6~/DACK3~	Not required
Mictor C pin 28	C0:5	NMI~	Not required
Mictor C pin 26	C0:6	PORESET~	Required
Mictor C pin 24	C0:7	GBL~	Not required
Mictor C pin 22	C1:0	SRESET~	Required

Table 3-28: CPU to Mictor connections for Mictor C pins for 8101_SNG support (cont.)

AMP mictor pin number	Logic analyzer acquisition channel	MSC8101 support package channel name	Required/Not required for disassembly
Mictor C pin 20	C1:1	HRESET~	Required
Mictor C pin 18	C1:2	NMI_OUT~	Not required
Mictor C pin 16	C1:3	BCTL0~	Not required
Mictor C pin 14	C1:4	PSDAMUX	Not required
Mictor C pin 12	C1:5	PGTA~	Not required
Mictor C pin 10	C1:6	PSDA10	Required
Mictor C pin 08	C1:7	PSDWE~	Required
Mictor C pin 06	QUAL:1	IRQ7~/INT_OUT~	Not required

Table 3-29: CPU to Mictor connections for Mictor D pins for 8101_SNG support

AMP mictor pin number	Logic analyzer acquisition channel	MSC8101 support package channel name	Required/Not required for disassembly
Mictor D pin 05	QUAL:0	CS2~	Required
Mictor D pin 07	D3:7	D32	Required
Mictor D pin 09	D3:6	D33	Required
Mictor D pin 11	D3:5	D34	Required
Mictor D pin 13	D3:4	D35	Required
Mictor D pin 15	D3:3	D36	Required
Mictor D pin 17	D3:2	D37	Required
Mictor D pin 19	D3:1	D38	Required
Mictor D pin 21	D3:0	D39	Required
Mictor D pin 23	D2:7	D40	Required
Mictor D pin 25	D2:6	D41	Required
Mictor D pin 27	D2:5	D42	Required
Mictor D pin 29	D2:4	D43	Required
Mictor D pin 31	D2:3	D44	Required
Mictor D pin 33	D2:2	D45	Required
Mictor D pin 35	D2:1	D46	Required
Mictor D pin 37	D2:0	D47	Required
Mictor D pin 38	D0:0	D63	Required
Mictor D pin 36	D0:1	D62	Required
Mictor D pin 34	D0:2	D61	Required
Mictor D pin 32	D0:3	D60	Required

Table 3-29: CPU to Mictor connections for Mictor D pins for 8101_SNG support (cont.)

AMP mictor pin number	Logic analyzer acquisition channel	MSC8101 support package channel name	Required/Not required for disassembly
Mictor D pin 30	D0:4	D59	Required
Mictor D pin 28	D0:5	D58	Required
Mictor D pin 26	D0:6	D57	Required
Mictor D pin 24	D0:7	D56	Required
Mictor D pin 22	D1:0	D55	Required
Mictor D pin 20	D1:1	D54	Required
Mictor D pin 18	D1:2	D53	Required
Mictor D pin 16	D1:3	D52	Required
Mictor D pin 14	D1:4	D51	Required
Mictor D pin 12	D1:5	D50	Required
Mictor D pin 10	D1:6	D49	Required
Mictor D pin 08	D1:7	D48	Required
Mictor D pin 06	CLOCK:2	CS3~	Required

Table 3-30: CPU to Mictor connections for Mictor E pins for 8101_SNG support

AMP mictor pin number	Logic analyzer acquisition channel	MSC8101 support package channel name	Required/Not required for disassembly
Mictor E pin 05	QUAL:3	CS0~	Required
Mictor E pin 07	E3:7	D0 (MSB)	Required
Mictor E pin 09	E3:6	D1	Required
Mictor E pin 11	E3:5	D2	Required
Mictor E pin 13	E3:4	D3	Required
Mictor E pin 15	E3:3	D4	Required
Mictor E pin 17	E3:2	D5	Required
Mictor E pin 19	E3:1	D6	Required
Mictor E pin 21	E3:0	D7	Required
Mictor E pin 23	E2:7	D8	Required
Mictor E pin 25	E2:6	D9	Required
Mictor E pin 27	E2:5	D10	Required
Mictor E pin 29	E2:4	D11	Required
Mictor E pin 31	E2:3	D12	Required
Mictor E pin 33	E2:2	D13	Required
Mictor E pin 35	E2:1	D14	Required

Table 3-30: CPU to Mictor connections for Mictor E pins for 8101_SNG support (cont.)

AMP mictor pin number	Logic analyzer acquisition channel	MSC8101 support package channel name	Required/Not required for disassembly
Mictor E pin 37	E2:0	D15	Required
Mictor E pin 38	E0:0	D31	Required
Mictor E pin 36	E0:1	D30	Required
Mictor E pin 34	E0:2	D29	Required
Mictor E pin 32	E0:3	D28	Required
Mictor E pin 30	E0:4	D27	Required
Mictor E pin 28	E0:5	D26	Required
Mictor E pin 26	E0:6	D25	Required
Mictor E pin 24	E0:7	D24	Required
Mictor E pin 22	E1:0	D23	Required
Mictor E pin 20	E1:1	D22	Required
Mictor E pin 18	E1:2	D21	Required
Mictor E pin 16	E1:3	D20	Required
Mictor E pin 14	E1:4	D19	Required
Mictor E pin 12	E1:5	D18	Required
Mictor E pin 10	E1:6	D17	Required
Mictor E pin 08	E1:7	D16	Required
Mictor E pin 06	QUAL:2	CS1~	Required

8101_MLT Support

Tables 3-31 through 3-34 show the mictor pin connections for the logic analyzer and the AMP mictors for the 8101_MLT support.

Table 3-31: CPU to Mictor connections for Mictor A pins for 8101_MLT support

AMP mictor pin number	Logic analyzer acquisition channel	MSC8101 support package channel name	Required/Not required for disassembly
Mictor A pin 05	CLOCK:0	PSDVAL~	Required
Mictor A pin 07	A3:7	A0 (MSB)	Required
Mictor A pin 09	A3:6	A1	Required
Mictor A pin 11	A3:5	A2	Required
Mictor A pin 13	A3:4	A3	Required
Mictor A pin 15	A3:3	A4	Required
Mictor A pin 17	A3:2	A5	Required
Mictor A pin 19	A3:1	A6	Required
Mictor A pin 21	A3:0	A7	Required
Mictor A pin 23	A2:7	A8	Required
Mictor A pin 25	A2:6	A9	Required
Mictor A pin 27	A2:5	A10	Required
Mictor A pin 29	A2:4	A11	Required
Mictor A pin 31	A2:3	A12	Required
Mictor A pin 33	A2:2	A13	Required
Mictor A pin 35	A2:1	A14	Required
Mictor A pin 37	A2:0	A15	Required
Mictor A pin 38	A0:0	BADDR31/A31*	Required
Mictor A pin 36	A0:1	BADDR30/A30*	Required
Mictor A pin 34	A0:2	BADDR29/A29*	Required
Mictor A pin 32	A0:3	BADDR28/A28*	Required
Mictor A pin 30	A0:4	BADDR27A27*	Required
Mictor A pin 28	A0:5	A26	Required
Mictor A pin 26	A0:6	A25	Required
Mictor A pin 24	A0:7	A24	Required
Mictor A pin 22	A1:0	A23	Required
Mictor A pin 20	A1:1	A22	Required
Mictor A pin 18	A1:2	A21	Required
Mictor A pin 16	A1:3	A20	Required
Mictor A pin 14	A1:4	A19	Required
Mictor A pin 12	A1:5	A18	Required

Table 3-31: CPU to Mictor connections for Mictor A pins for 8101_MLT support (cont.)

AMP mictor pin number	Logic analyzer acquisition channel	MSC8101 support package channel name	Required/Not required for disassembly
Mictor A pin 10	A1:6	A17	Required
Mictor A pin 08	A1:7	A16	Required
Mictor A pin 06	CLOCK:1	CLKOUT	Required

* **You can trigger on Burst Address increments only if BADDR[31-27] is connected to logic analyzer channels A0:[0-4]. For more details, refer to *Triggering on Address in a Burst Transaction* on page 1-2.**

Table 3-32: CPU to Mictor connections for Mictor C pins for 8101_MLT support

AMP mictor pin number	Logic analyzer acquisition channel	MSC8101 support package channel name	Required/Not required for disassembly
Mictor C pin 05	CLOCK:3	TS~	Required
Mictor C pin 07	C3:7	CS4~	Required
Mictor C pin 09	C3:6	ABB~	Required
Mictor C pin 11	C3:5	BG~	Required
Mictor C pin 13	C3:4	DP0~/EXT_BR2~	Not required
Mictor C pin 15	C3:3	CS5~	Required
Mictor C pin 17	C3:2	BR~	Not required
Mictor C pin 19	C3:1	ALE	Required
Mictor C pin 21	C3:0	DBG~	Required
Mictor C pin 23	C2:7	DBB~	Required
Mictor C pin 25	C2:6	TC2/DBG0~*	Required
Mictor C pin 27	C2:5	DP3~/EXT_BR3~	Not required
Mictor C pin 29	C2:4	CS6~	Required
Mictor C pin 31	C2:3	CS7~	Required
Mictor C pin 33	C2:2	DP1~/EXT_BG2~	Required
Mictor C pin 35	C2:1	DP2~/EXT_DBG2~	Required
Mictor C pin 37	C2:0	DP4~/EXT_BG3~	Required
Mictor C pin 38	C0:0	TC1/BG0~*	Required
Mictor C pin 36	C0:1	TC0/BR0~*	Required for Internal Arbiter Mode Not Required for External Arbiter Mode
Mictor C pin 34	C0:2	TEA~	Required
Mictor C pin 32	C0:3	TA~	Required
Mictor C pin 30	C0:4	TT4	Required

Table 3-32: CPU to Mictor connections for Mictor C pins for 8101_MLT support (cont.)

AMP mictor pin number	Logic analyzer acquisition channel	MSC8101 support package channel name	Required/Not required for disassembly
Mictor C pin 28	C0:5	TT3	Required
Mictor C pin 26	C0:6	TT2	Required
Mictor C pin 24	C0:7	TT1	Required
Mictor C pin 22	C1:0	TT0	Required
Mictor C pin 20	C1:1	TSIZ3	Required
Mictor C pin 18	C1:2	TSIZ2	Required
Mictor C pin 16	C1:3	TSIZ1	Required
Mictor C pin 14	C1:4	TSIZ0	Required
Mictor C pin 12	C1:5	DP5~/EXT_DBG3~	Required
Mictor C pin 10	C1:6	ARTRY~	Required
Mictor C pin 08	C1:7	TBST~	Required
Mictor C pin 06	QUAL:1	AACK~	Required

* **When you use the 8101_MLT support for Internal Arbiter configuration, connect the signals TC0-TC2 to C0:0, C0:0, and C2:6. For External Arbiter configuration, connect the signals BR0~, BG0~, and DBG0~ (request and grant signals from the fourth external master that is connected to the bus) to C0:1, C0:0, and C2:6.**

Table 3-33: CPU to Mictor connections for Mictor D pins for 8101_MLT support

AMP mictor pin number	Logic analyzer acquisition channel	MSC8101 support package channel name	Required/Not required for disassembly
Mictor D pin 05	QUAL:0	CS2~	Required
Mictor D pin 07	D3:7	D32	Required
Mictor D pin 09	D3:6	D33	Required
Mictor D pin 11	D3:5	D34	Required
Mictor D pin 13	D3:4	D35	Required
Mictor D pin 15	D3:3	D36	Required
Mictor D pin 17	D3:2	D37	Required
Mictor D pin 19	D3:1	D38	Required
Mictor D pin 21	D3:0	D39	Required
Mictor D pin 23	D2:7	D40	Required
Mictor D pin 25	D2:6	D41	Required
Mictor D pin 27	D2:5	D42	Required
Mictor D pin 29	D2:4	D43	Required
Mictor D pin 31	D2:3	D44	Required

Table 3-33: CPU to Mictor connections for Mictor D pins for 8101_MLT support (cont.)

AMP mictor pin number	Logic analyzer acquisition channel	MSC8101 support package channel name	Required/Not required for disassembly
Mictor D pin 33	D2:2	D45	Required
Mictor D pin 35	D2:1	D46	Required
Mictor D pin 37	D2:0	D47	Required
Mictor D pin 38	D0:0	D63	Required
Mictor D pin 36	D0:1	D62	Required
Mictor D pin 34	D0:2	D61	Required
Mictor D pin 32	D0:3	D60	Required
Mictor D pin 30	D0:4	D59	Required
Mictor D pin 28	D0:5	D58	Required
Mictor D pin 26	D0:6	D57	Required
Mictor D pin 24	D0:7	D56	Required
Mictor D pin 22	D1:0	D55	Required
Mictor D pin 20	D1:1	D54	Required
Mictor D pin 18	D1:2	D53	Required
Mictor D pin 16	D1:3	D52	Required
Mictor D pin 14	D1:4	D51	Required
Mictor D pin 12	D1:5	D50	Required
Mictor D pin 10	D1:6	D49	Required
Mictor D pin 08	D1:7	D48	Required
Mictor D pin 06	CLOCK:2	CS3~	Required

Table 3-34: CPU to Mictor connections for Mictor E pins for 8101_MLT support

AMP mictor pin number	Logic analyzer acquisition channel	MSC8101 support package channel name	Required/Not required for disassembly
Mictor E pin 05	QUAL:3	CS0~	Required
Mictor E pin 07	E3:7	D0 (MSB)	Required
Mictor E pin 09	E3:6	D1	Required
Mictor E pin 11	E3:5	D2	Required
Mictor E pin 13	E3:4	D3	Required
Mictor E pin 15	E3:3	D4	Required
Mictor E pin 17	E3:2	D5	Required
Mictor E pin 19	E3:1	D6	Required
Mictor E pin 21	E3:0	D7	Required

Table 3-34: CPU to Mictor connections for Mictor E pins for 8101_MLT support (cont.)

AMP mictor pin number	Logic analyzer acquisition channel	MSC8101 support package channel name	Required/Not required for disassembly
Mictor E pin 23	E2:7	D8	Required
Mictor E pin 25	E2:6	D9	Required
Mictor E pin 27	E2:5	D10	Required
Mictor E pin 29	E2:4	D11	Required
Mictor E pin 31	E2:3	D12	Required
Mictor E pin 33	E2:2	D13	Required
Mictor E pin 35	E2:1	D14	Required
Mictor E pin 37	E2:0	D15	Required
Mictor E pin 38	E0:0	D31	Required
Mictor E pin 36	E0:1	D30	Required
Mictor E pin 34	E0:2	D29	Required
Mictor E pin 32	E0:3	D28	Required
Mictor E pin 30	E0:4	D27	Required
Mictor E pin 28	E0:5	D26	Required
Mictor E pin 26	E0:6	D25	Required
Mictor E pin 24	E0:7	D24	Required
Mictor E pin 22	E1:0	D23	Required
Mictor E pin 20	E1:1	D22	Required
Mictor E pin 18	E1:2	D21	Required
Mictor E pin 16	E1:3	D20	Required
Mictor E pin 14	E1:4	D19	Required
Mictor E pin 12	E1:5	D18	Required
Mictor E pin 10	E1:6	D17	Required
Mictor E pin 08	E1:7	D16	Required
Mictor E pin 06	QUAL:2	CS1~	Required

Specifications

Specifications

This section contains the specifications for the support.

Specification Tables

Table 4–1 lists the electrical requirements the target system must produce for the support to acquire correct data.

Table 4-1: Electrical specifications

Characteristics	Requirements
Target system clock rate	
8101_SNG specified clock rate	Maximum 100 MHz
8101_SNG tested clock rate	Maximum 50 MHz
8101_MLT specified clock rate	Maximum 100 MHz
8101_MLT tested clock rate	Maximum 66 MHz
Minimum setup time required	2.5 ns
Minimum hold time required	0 ns

Replaceable Parts List

Replaceable Parts Lists

This section contains a list of the replaceable components and modules for the TMS708 MSC8101 support. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Using the Replaceable Parts List

The tabular information in the Replaceable Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes the content of each column in the parts list.

Parts list column descriptions

Column	Column name	Description
1	Figure & index number	Items in this section are referenced by figure and index numbers to the exploded view illustrations that follow.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entry indicates the part is good for all serial numbers.
5	Qty	This indicates the quantity of parts used.
6	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
7	Mfr. code	This indicates the code of the actual manufacturer of the part.
8	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Chassis Parts

Chassis-mounted parts and cable assemblies are located at the end of the Replaceable Parts List.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
80009	TEKTRONIX, INC.	P.O. BOX 500	BEAVERTON, OR, 97077-0001

Replaceable parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
					STANDARD ACCESSORIES		
	071-1117-00			1	MANUAL,TECH INSTRUCTIONS,MSC8101;TMS708	80009	071-1117-00

Index

Index

F

H

I

L

M

N

O

P

Q

R

S

T

U

V

W